Hall Ticket Number:

Code No. : 21602

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

M.E. (ECE: CBCS) I-Semester Main Examinations, January-2018

(Embedded Systems & VLSI Design)

Digital IC Design

Time: **3** hours Max. Marks: **60**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

1. Explain MOSFET second order effects.
2. Find Propagation Delay of a CMOS inverter modelled as a First-Order RC Network (Assume 250 nm technology).
3. Explain charge leakage problem in dynamic CMOS circuits.
4. Implement 4×1 mux using transmission gate logic.
5. Compare PLL and DLL in VLSI Clock circuits.
6. Draw and explain circuit diagram of Simplified TSPC latch.
7. Discuss design challenges in power distribution in VLSI systems.
8. Implement 2 bit comparator using 1 bit comparator.
9. Draw and explain the circuit diagram of a 4T SRAM cell.
10. Estimate the LE of a CMOS NAND4.

Part-B (5 × 8 = 40 Marks)

11. a) For the inverter of Figure 1 and an output load of 3 pF: Compute the static and dynamic power dissipation assuming the gate is clocked as fast as possible. [5]

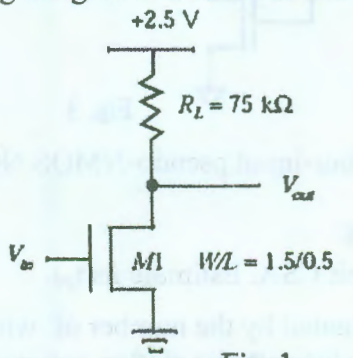

Fig. 1

b) Assume a wafer size of 12 inch, a die size of 2.5 cm^2, 1 defects/cm2, and α=3. Determine the die yield of this CMOS process run. [3]

12. a) Consider the two input NAND gate and assume NMOS and PMOS devices of 0.5µm / 0.25µm and 0.75µm/0.25µm, respectively. Find rise time and fall time this sizing should result in approximately equal worst-case rise and fall times. [5]

b) Implement XOR and XNOR using Complementary pass-transistor logic (CPL). [3]

13. a) Explain Design Techniques–dealing with Capacitive Cross Talk. [3]

b) Implement a 200 MHz current starved ring oscillator using not more than 11 stages. Estimate the Control voltage. [5]

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14. a) Implement a 16 bit Carry Save adder and estimate its propagation delay. [5]

    b) Show how the arithmetic module in Figure 2 can be used as a comparator. [3]

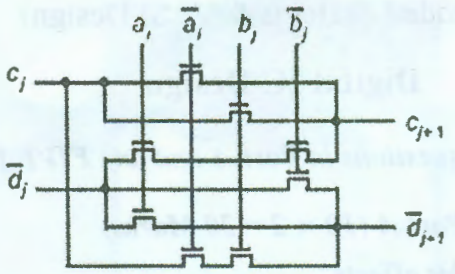

Fig. 2

15. a) Estimate the word-line and bit-line capacitances of a 512 Kb SRAM arranged as a 1024 × 512 array with access transistors of size (0.5μ/0.1μ). Assume wire cap = 0.3fF/μ, bit line (contact) cap = 0.5 fF, Transistor D/S cap = Gate cap = 2 fF/μ, and Cell size is 50λ × 40λ. Use 0.13μ technology and 1μ = 20λ. [5]

    b) Explain write and read operations in a 3T DRAM cell. [3]

16. a) The inverter in Figure 3 operates with V_{DD}=0.4V and is composed of |Vt| = 0.5V devices. The devices have identical I_0 and n, calculate the switching threshold (VM) of this inverter. [5]

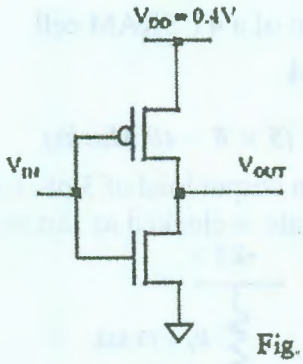

Fig. 3

    b) Draw the circuit diagram of four-input pseudo-NMOS NOR and NAND gates. [3]

17. Answer any ***two*** of the following:

    a) Explain the function of a 16 bit CSA. Estimate its t_{pd}. [4]

    b) The layout of shifters is dominated by the number of wires running through a cell. For both the barrel shifter and the logarithmic shifter, estimate the width of a shifter cell as a function of the maximum shift-width M and the metal pitch p. [4]

    c) Design a Row decoder to select one out of 16 bit lines based on address bits A3, A2, A1, and A0 and their complements. Compare its performance without a pre-decoder. [4]